6.1 A 16mA UWB 3-to-5GHz 20Mpulses/s Quadrature Analog Correlation Receiver in 0.18μm CMOS

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Ultra-wideband (UWB) technology based on impulse radio (IR) is a strong candidate for wireless sensor network applications [1]. The low data rates required by these applications have focused a great deal of attention on low-complexity sub-optimal solutions where baseline power consumption is reduced. The UWB-IR results from a compromise between power consumption and implementation complexity. However UWB-IR usually suffers from limited flexibility in defining the spectrum for multiple-access or to satisfy the UWB spectral mask. Therefore the carrier-based IR (CB-IR) approach has been proposed as an alternative signal scheme for sufficient flexibility while keeping the system complexity as low as possible [2]. In this paper we demonstrate a receiver that is suitable for most IR approaches and is especially convenient for the CB-IR. The receiver architecture (Fig. 6.1.1) is a direct down-conversion architecture with analog quadrature correlator. A downconverted CB-IR signal has a bandwidth that still spans a few hundreds of MHz. The digital processing of such signals usually requires a fast-sampling ADC and a high-frequency clock generator. Here, the complete pulse correlation is realized in the analog domain such that the sampling can be done at the pulse rate. Since the receiver features pulse-position modulation (PPM), one sample is taken at each possible position.

The receiver front-end comprises an LNA and two quadrature down-conversion mixers (I and Q paths). In order to reuse bias current, the LNA and the mixers are stacked above each other [3] as shown in Fig. 6.1.2. The circuit provides differential 50Ω input matching from 3 to 5GHz through two consecutive *LC* stages. A cascode transistor isolates the LNA from the I and Q switching differential pairs. A common-mode feedback loop is implemented to stabilize dc common-mode voltage at the mixer output. The LNA-mixer combination provides less than -10dB input reflection coefficient in-band and 24dB gain with a 7.5dB cascaded noise figure over the whole band. An on-chip free-running tunable three-stage ring oscillator provides the local oscillator (LO). The LO center frequency drift is much smaller than the bandwidth of UWB signals, so the signal power spectrum remains in the reception window while the phase rotation is captured by the quadrature projection. The three 120° outputs are recombined into quadrature LO tones (Fig. 6.1.2). The I and Q baseband outputs of the mixers are filtered for channel selection through a 3rd-order active filter [4] with variable gain (nominal value 0 to 15dB) and variable bandwidth (nominal value 250MHz to 1GHz). It exploits the low linearity requirement in using a stacked MOS-C structure, which allows a 3rd-order transfer function to be synthesized in a single path. The power consumption is low, ranging from 210μW (for 0dB@250MHz) to 3.2mW (for 15dB@1GHz).

Analog correlation is realized by matched filtering with a rectangular template using a switcheable integrator circuit. The output is taken by a 4b ADC precisely triggered by a digitally-contolled timing circuit (TC). In the integrator circuit, positive feedback in the load enables dc-gain in excess of 60dB with a unity-gain bandwidth of 1GHz, while consuming 120μW [4] (no stability issue is present since it is operating open loop). Two PMOS current sources are also added to remove the dc offset at the integrator input. The differential 4b ADC consists of 15 comparator stages, a set-reset latch array and a ROM-based Gray level encoder. Significantly downsizing the transistors and using calibration to cope with the increased mismatch errors have reduced its power consumption. A SNDR higher than 22dB is measured up to 700MHz (Fig. 6.1.3). This 3.5ENOB ADC consumes a measured 1pJ/conversion-step when running at 80MS/s. The TC is responsible for the generation of multi-phased signals that enable/disable the operation of the analog blocks. The TC consists of two serially cascaded delay lines, the first for the PPM delay and the second for setting the required time window to enable the operation of the analog block under consideration within the pulse frame (Fig. 6.1.4). The input to the TC is the system clock, synchronized to the pulse repetition frequency. An on-chip variable delay line controls the phase of the system clock to align it to the phase of the transmitter clock. The variable delay line comprises two stages, one for coarse delay steps (1ns steps measured) and one for fine delay steps (60ps steps measured). The delay line guarantees that the new delay value becomes active at the times when no edge is present at the resulting output clock. The minimum pulse width of the clock is guaranteed to be 4ns, so that no glitch occurs at the clock output. The front-end settings, such as the correlation window length, the ADC calibration data and the output sampled data values from the ADC, are managed by an on-chip central controller that interfaces with either a PC or an FPGA through a high-speed bus.

The analog outputs from the integrator have been brought off-chip for measurement (Fig. 6.1.1) and are shown in Fig. 6.1.5. The integrated correlation energy is shown on the top of the figure for a PPM-modulated pulse stream. The bottom of the figure shows a close-up view of two consecutive pulses. The total current consumption of the chip including the digital baseband is 16mA measured with a 1.8V supply and a 20MHz clock rate. The measured break-down of the power consumption is given in Fig. 6.1.6 together with the performance summary. The receiver is fully integrated in a 0.18μm CMOS technology. A chip micrograph is shown in Fig. 6.1.7.

A fully integrated low-power UWB receiver is demonstrated in this paper. It operates between 3 and 5GHz and can process pulses with 500MHz to 2GHz bandwidth thanks to a variable channel select filter. Although the receiver is demonstrated for a PPM modulated pulse stream, the separate I and Q correlation energy can also be used to demodulate BPSK pulses at the expense of locking the oscillator in a control loop. This receiver demonstrates the potential of IR-UWB for low data rate sensor network applications.

Acknowledgments:
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[4] S. D'Amico et al., "A up to 1GHz Low-Power Continuous-Time '3rd-Order Filter+Integrator' Chain for Wireless Body-Area Network Receivers," *IEEE Prime*, Lausanne (Switzerland), 2005.

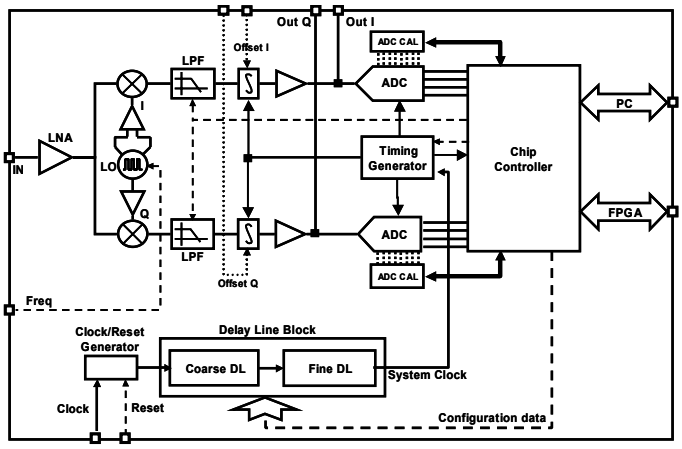

Figure 6.1.1: Architecture of the quadrature analog correlation receiver.

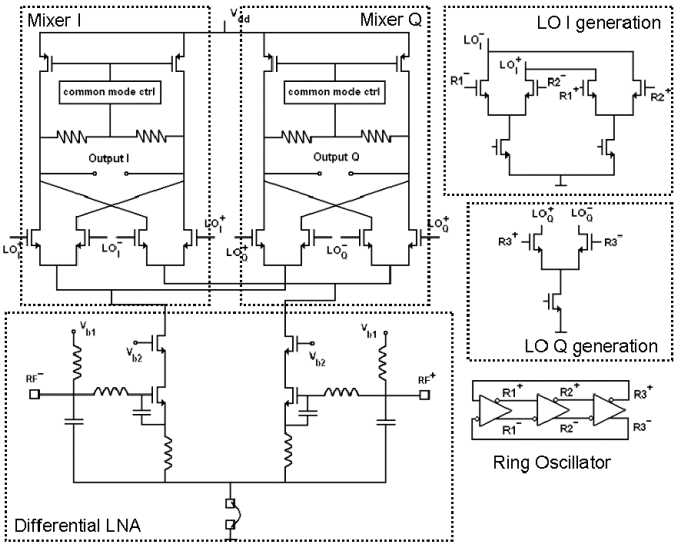

Figure 6.1.2: LNA-mixer combination with I and Q LO generation.

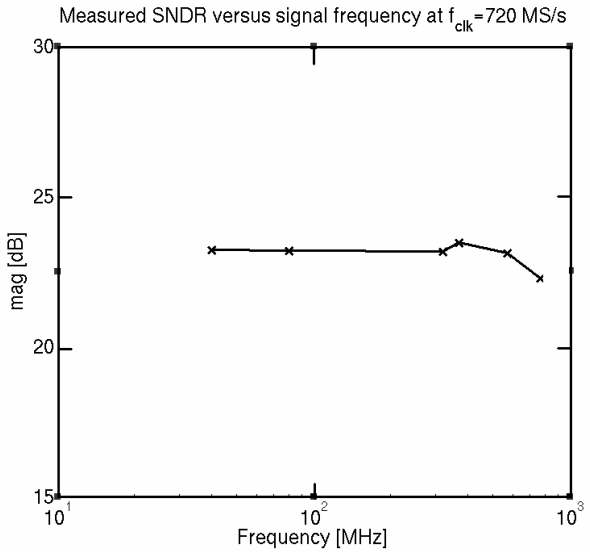

Figure 6.1.3: Measured SNDR of the ADC as a function of the input frequency.

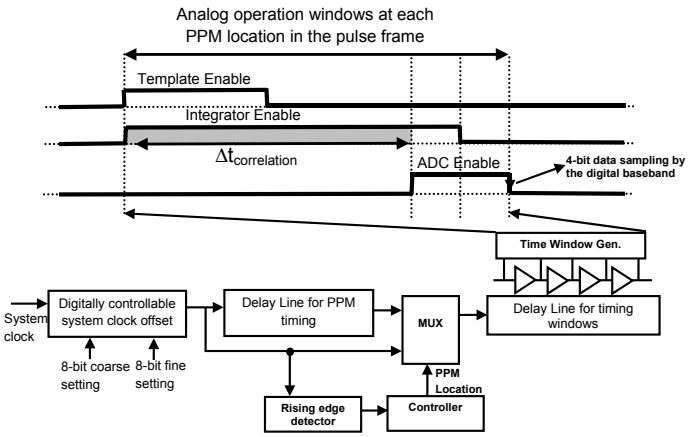

Figure 6.1.4: Timing generation module that controls the timing of the analog block's operation windows.

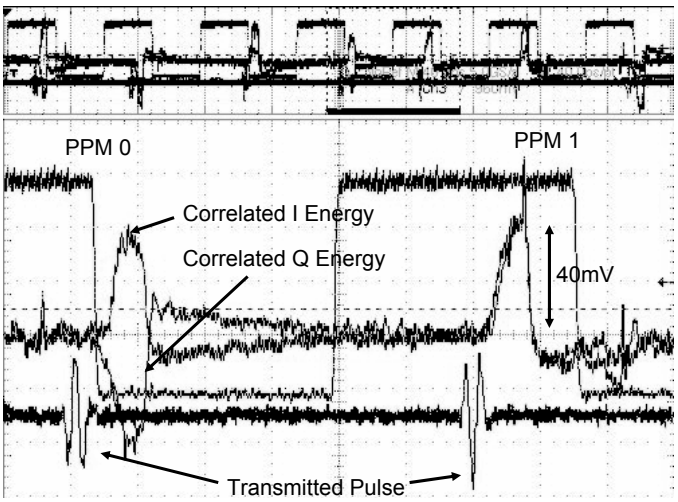

Figure 6.1.5: Measured correlator energy before ADC sampling. A subsampled version of the transmitted pulse train is also shown.

Front-End	Gain	**25dB**
	NF	**8dB**
	S11	**<10dB**
Baseband Filter	cut-off	**250-1000MHz**
	gain	**0-15dB**
Integrator	UGB	**1GHz**
	DC gain	**>60dB**
Timing Generator	Pulse width	**0.8-4.2ns**
	PPM Pulse position	**8-22ns**
ADC	ENOB	**3.5**
Delay Line	Coarse steps	**1ns**
	Fine steps	**60ps**
Power consumption @ 20MHz clock	LNA+Mixer	**4.9mA**
	LO generation	**7.5mA**
	Analog Baseband	**1.8mA**
	ADC (I+Q)	**0.45mA**
	Digital	**0.72-1.12mA**
	Total	**~16mA**

Figure 6.1.6: Table summary of receiver characteristics.

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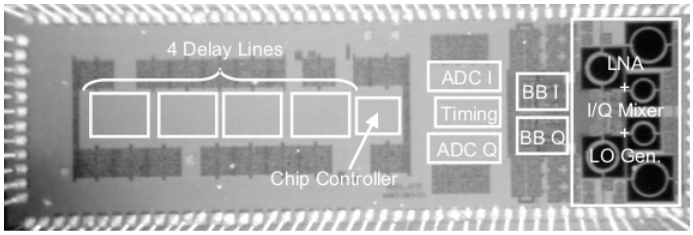

Figure 6.1.7: Chip micrograph of the receiver designed in CMOS 0.18µm technology. The die size is 5.0×1.6mm².

